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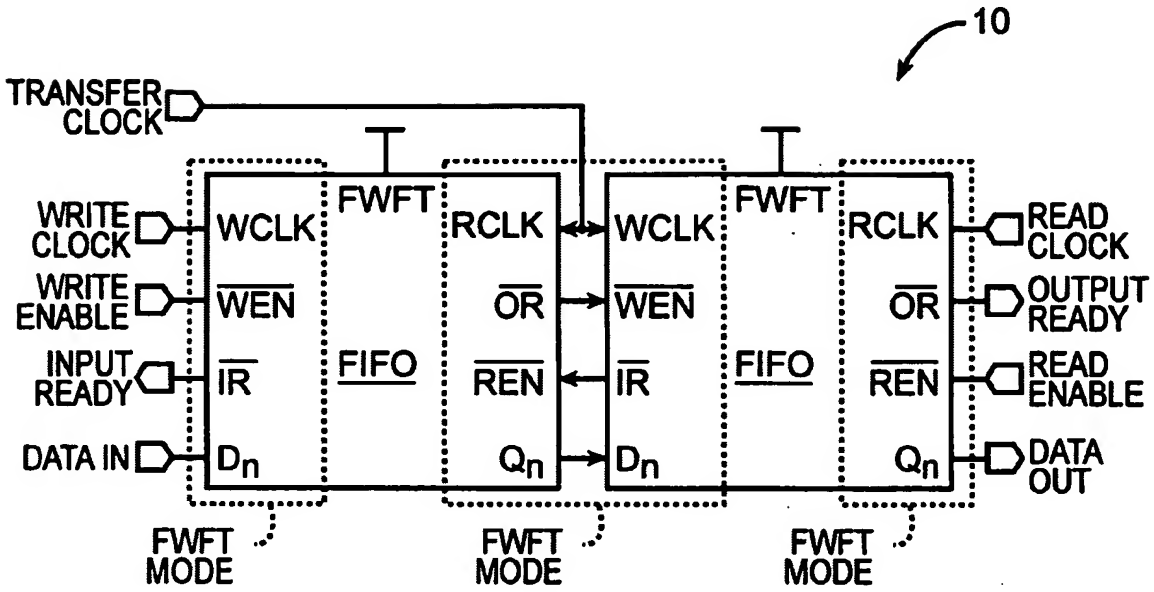


FIG. 1A
(PRIOR ART)

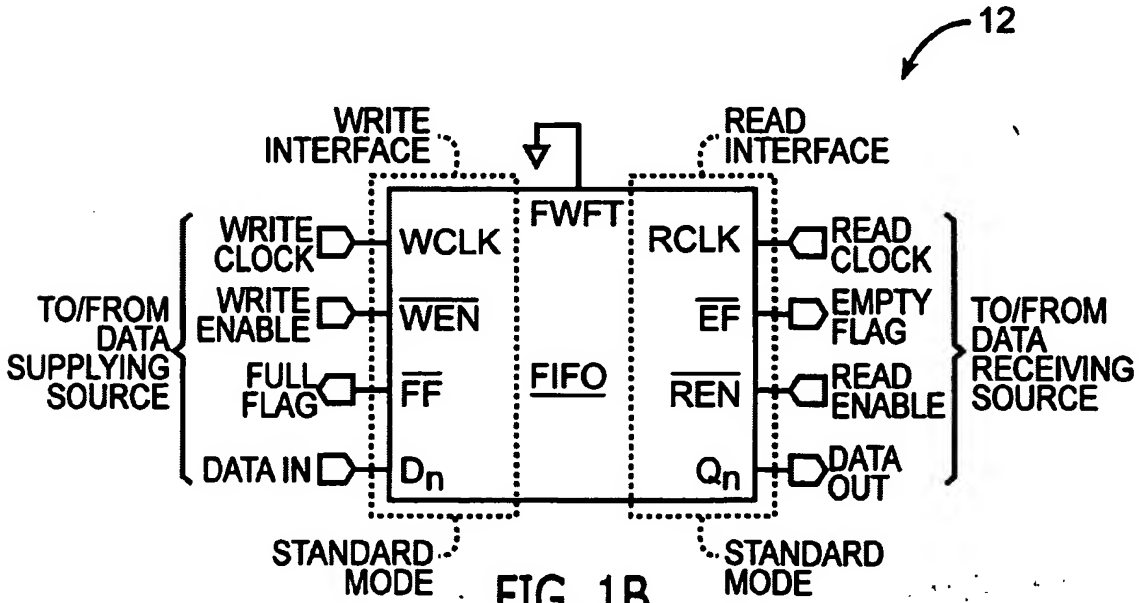


FIG. 1B
(PRIOR ART)

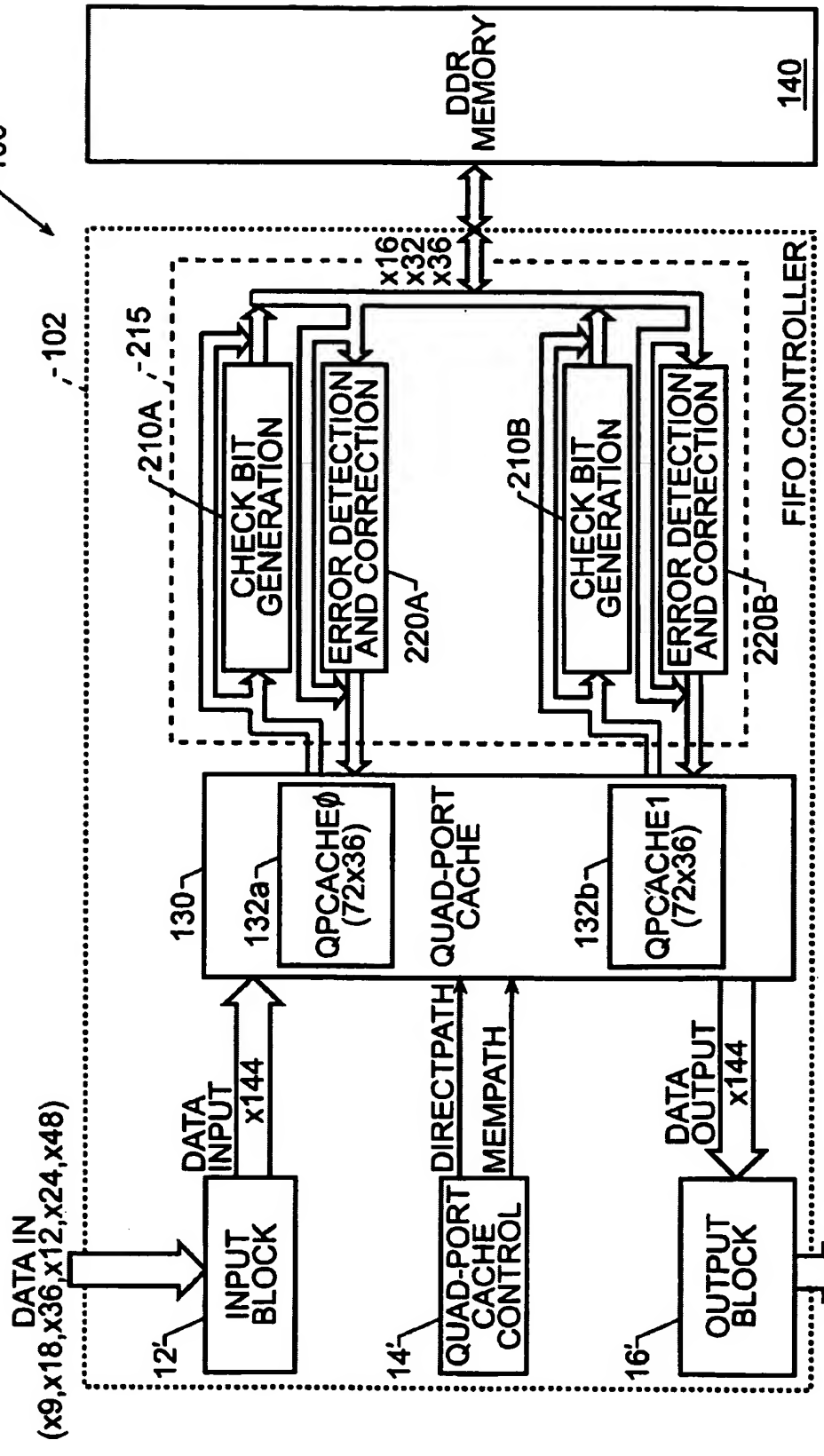

100
DDR MEMORY
140
102
215
x16
x32
x36
210A
210B
CHECK BIT GENERATION
ERROR DETECTION AND CORRECTION
220A
220B
FIFO CONTROLLER
130
132a
QPCACHEϕ (72x36)
QUAD-PORT CACHE
132b
QPCACHE1 (72x36)
DATA INPUT
x144
DIRECTPATH
MEMPATH
DATA OUTPUT
x144
DATA IN (x9,x18,x36,x12,x24,x48)
12'
INPUT BLOCK
14'
QUAD-PORT CACHE CONTROL
16'
OUTPUT BLOCK
DATA OUT (x9,x18,x36,x12,x24,x48)

FIG. 2

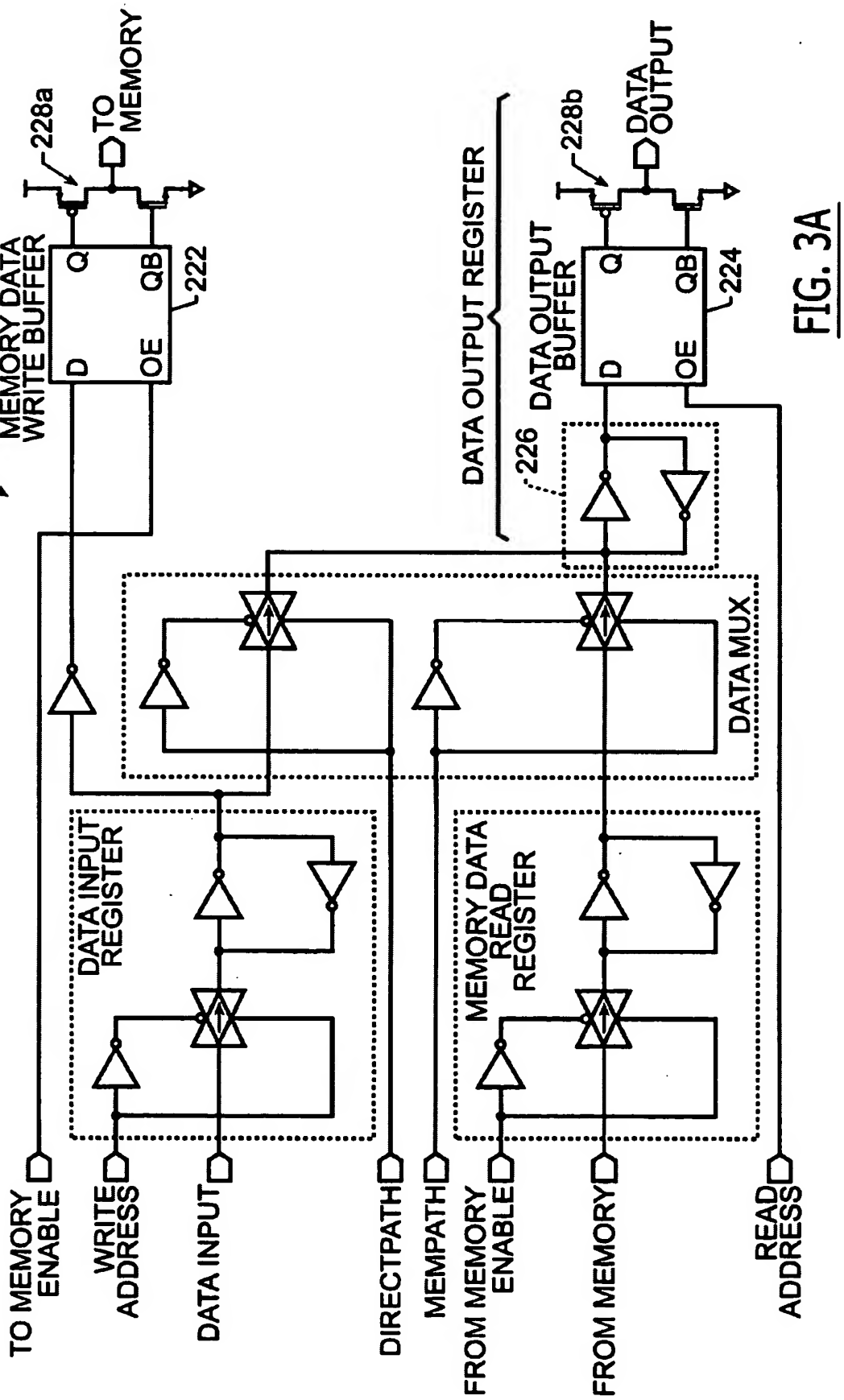

130a
MEMORY DATA WRITE BUFFER
222
228a
TO MEMORY
DATA OUTPUT REGISTER
DATA OUTPUT BUFFER
224
228b
DATA OUTPUT
226
DATA MUX
DATA INPUT REGISTER
MEMORY DATA READ REGISTER
TO MEMORY ENABLE
WRITE ADDRESS
DATA INPUT
DIRECTPATH
MEMPATH
FROM MEMORY ENABLE
FROM MEMORY
READ ADDRESS

FIG. 3A

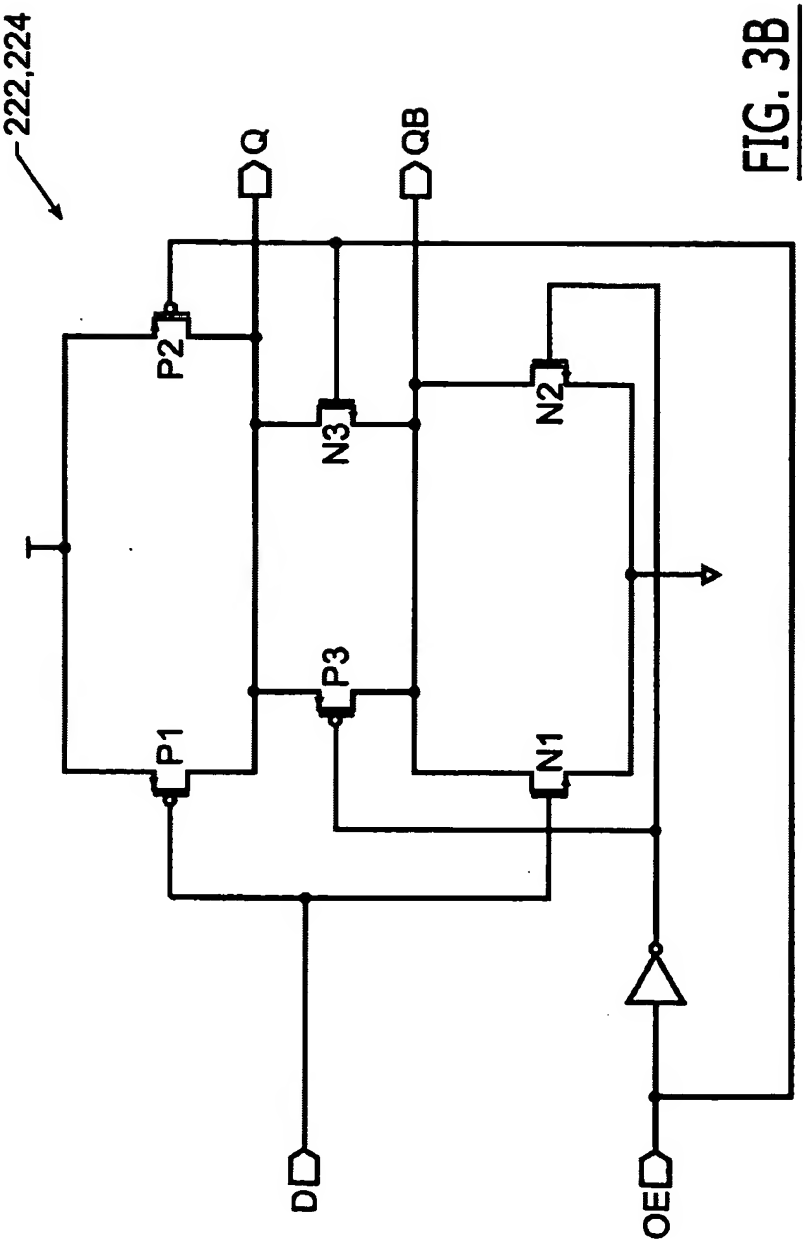


FIG. 3B

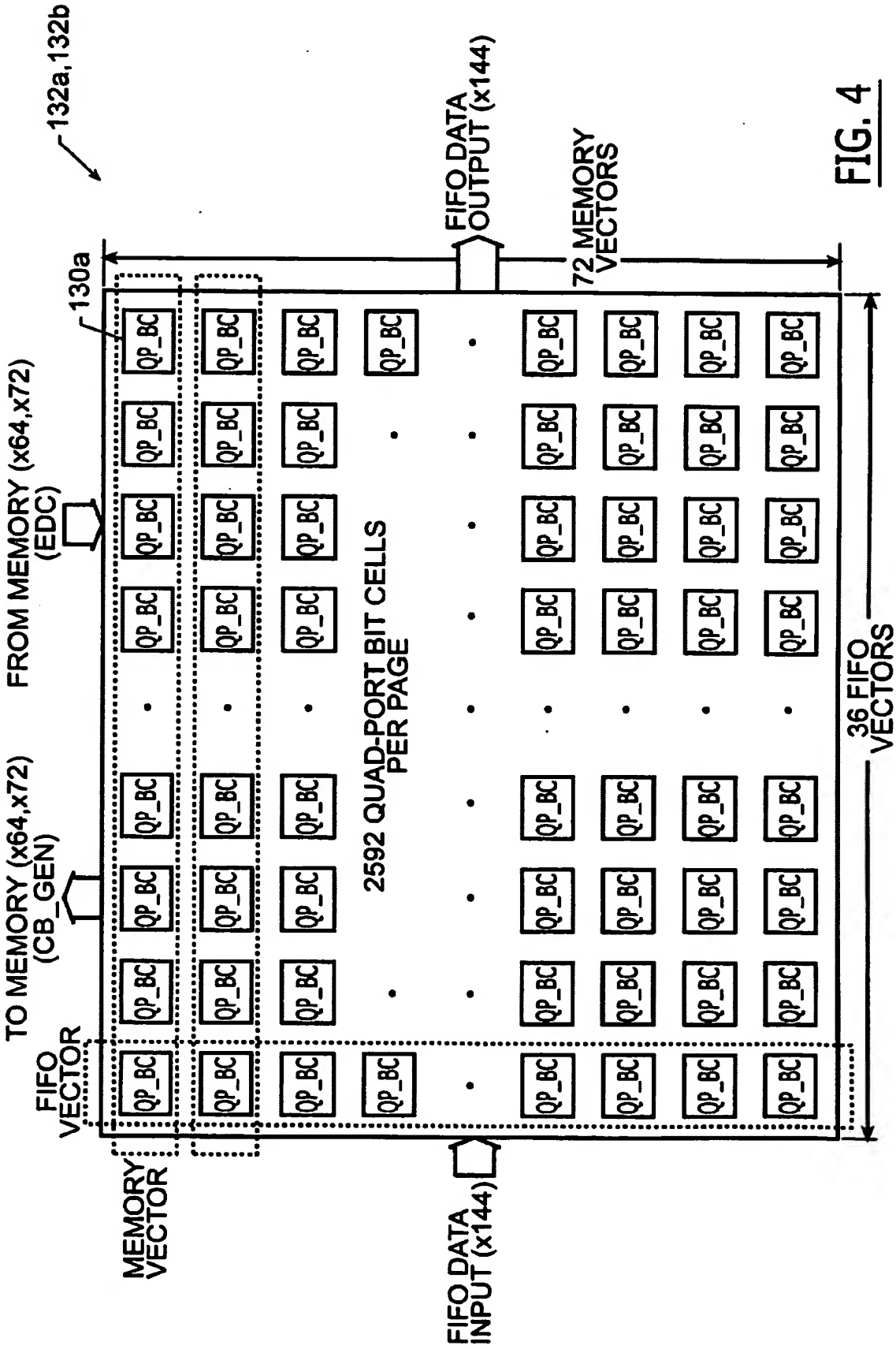

132a,132b
130a
FROM MEMORY (x64,x72)
(EDC)
TO MEMORY (x64,x72)
(CB_GEN)
FIFO
VECTOR
MEMORY
VECTOR
FIFO DATA
INPUT (x144)
FIFO DATA
OUTPUT (x144)
72 MEMORY
VECTORS
36 FIFO
VECTORS
2592 QUAD-PORT BIT CELLS
PER PAGE
QP_BC

FIG. 4

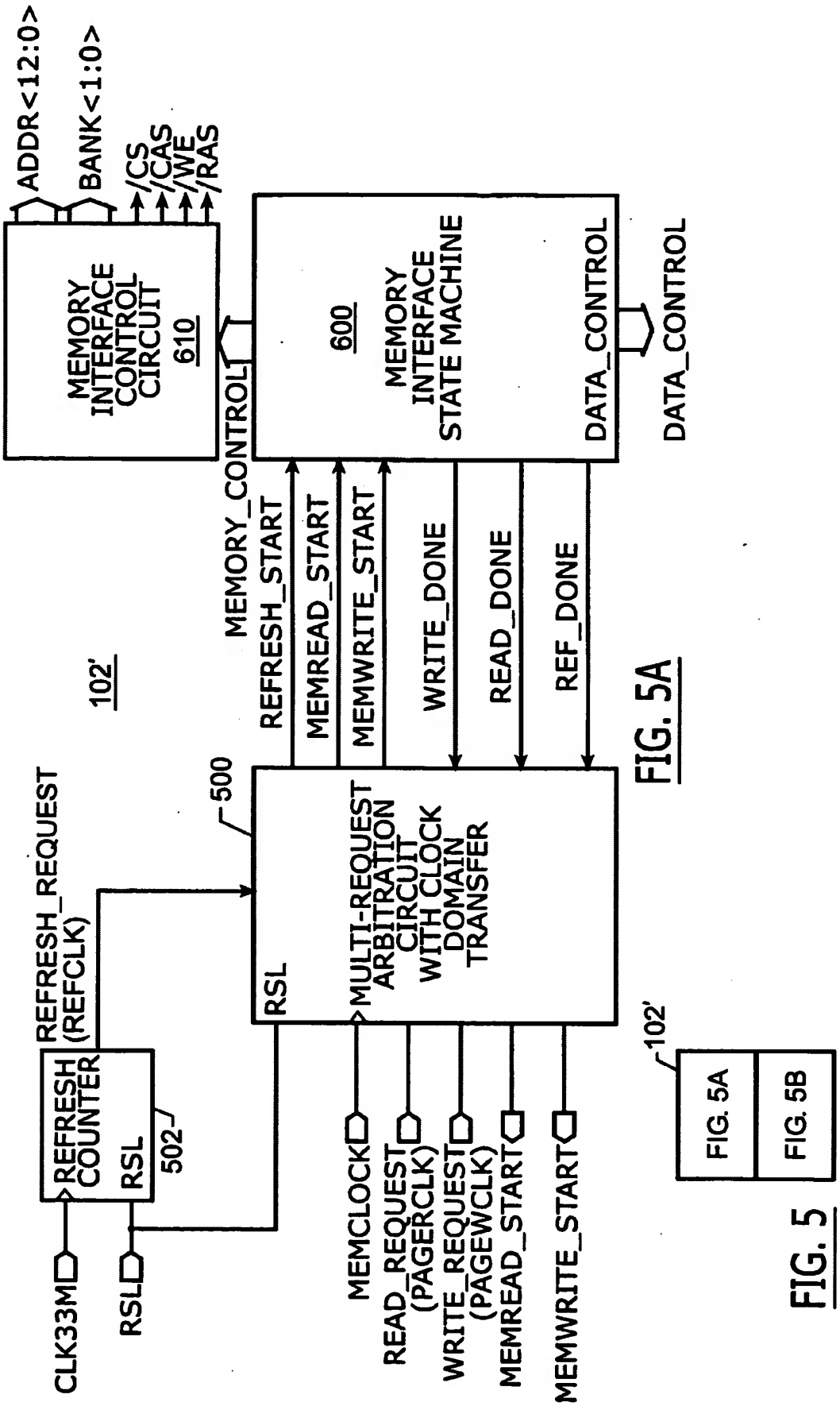

ADDR<12:0>
BANK<1:0>
/CS
/CAS
/WE
/RAS
MEMORY INTERFACE CONTROL CIRCUIT
610
600
MEMORY INTERFACE STATE MACHINE
MEMORY_CONTROL
DATA_CONTROL
DATA_CONTROL
REFRESH_START
MEMREAD_START
MEMWRITE_START
WRITE_DONE
READ_DONE
REF_DONE
102'
500
RSL
MULTI-REQUEST ARBITRATION CIRCUIT WITH CLOCK DOMAIN TRANSFER
REFRESH_REQUEST (REFCLK)
REFRESH COUNTER
RSL
502
CLK33M
RSL
MEMCLOCK
READ_REQUEST (PAGERCLK)
WRITE_REQUEST (PAGEWCLK)
MEMREAD_START
MEMWRITE_START
102'
FIG. 5A
FIG. 5B

FIG. 5A

FIG. 5

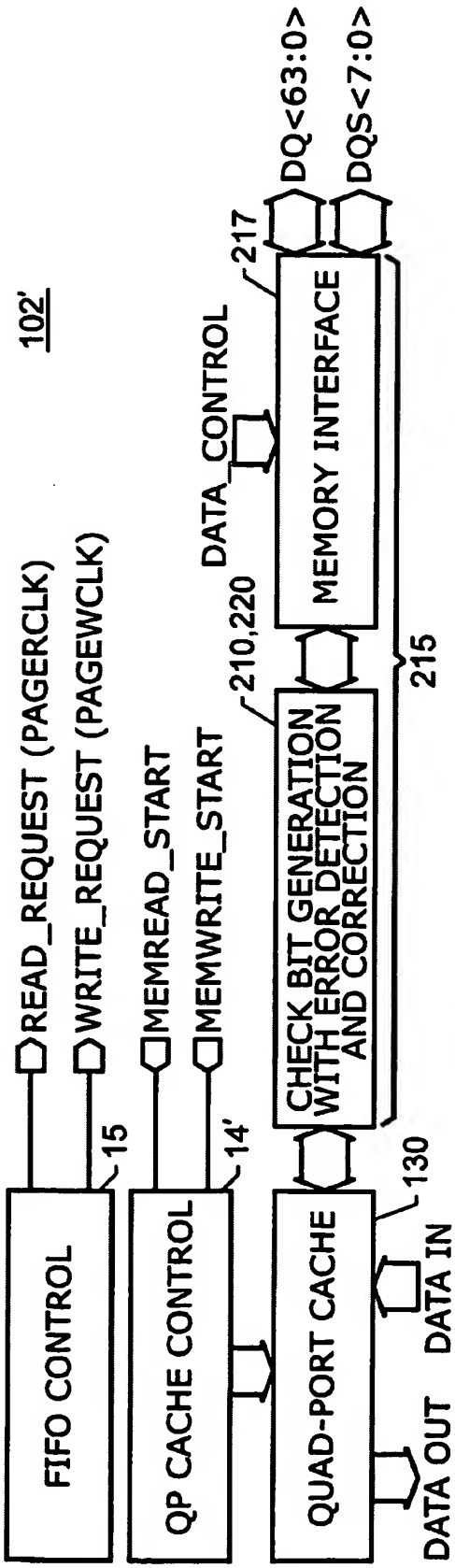
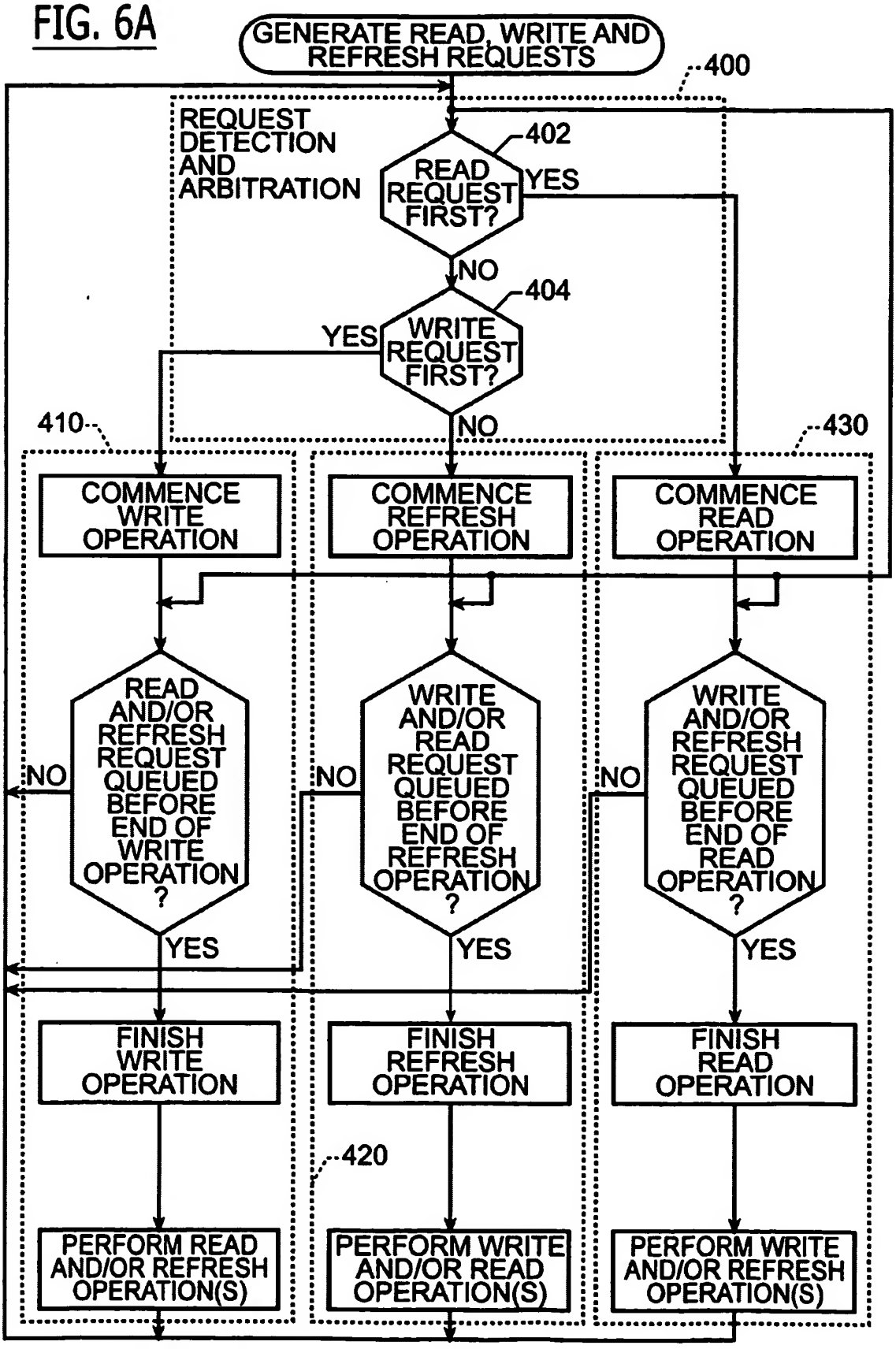

102'
READ_REQUEST (PAGERCLK)
WRITE_REQUEST (PAGEWCLK)
MEMREAD_START
MEMWRITE_START
DATA_CONTROL
DQ<63:0>
DQS<7:0>
217
210,220
215
15
14'
130
FIFO CONTROL
QP CACHE CONTROL
QUAD-PORT CACHE
CHECK BIT GENERATION WITH ERROR DETECTION AND CORRECTION
MEMORY INTERFACE
DATA OUT
DATA IN

FIG. 5B

FIG. 6A


GENERATE READ, WRITE AND REFRESH REQUESTS
400
REQUEST DETECTION AND ARBITRATION
402
READ REQUEST FIRST?
YES
NO
404
WRITE REQUEST FIRST?
YES
NO
410
430
COMMENCE WRITE OPERATION
COMMENCE REFRESH OPERATION
COMMENCE READ OPERATION
READ AND/OR REFRESH REQUEST QUEUED BEFORE END OF WRITE OPERATION ?
WRITE AND/OR READ REQUEST QUEUED BEFORE END OF REFRESH OPERATION ?
WRITE AND/OR REFRESH REQUEST QUEUED BEFORE END OF READ OPERATION ?
NO
NO
NO
YES
YES
YES
FINISH WRITE OPERATION
FINISH REFRESH OPERATION
FINISH READ OPERATION
420
PERFORM READ AND/OR REFRESH OPERATION(S)
PERFORM WRITE AND/OR READ OPERATION(S)
PERFORM WRITE AND/OR REFRESH OPERATION(S)

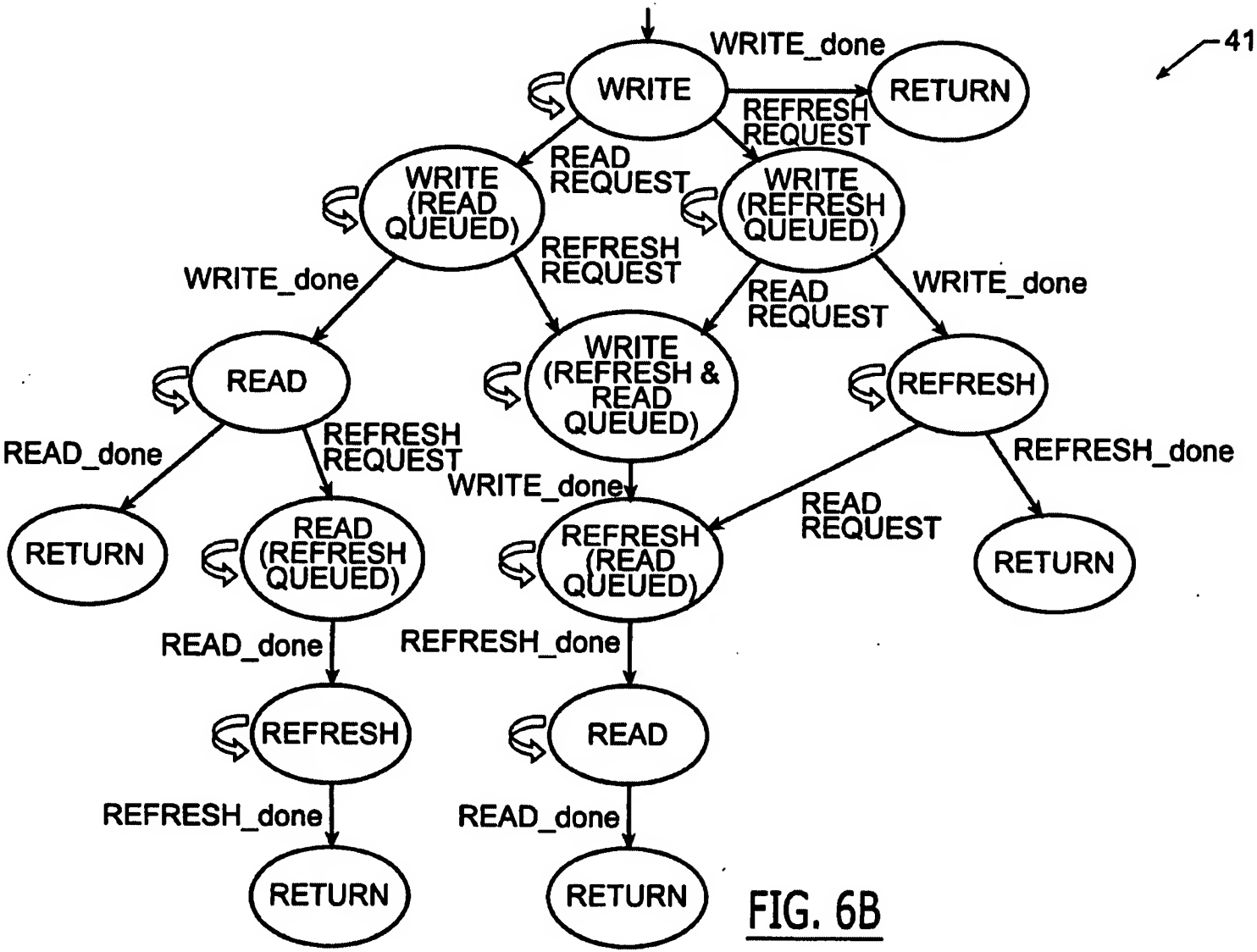


FIG. 6B

Replacement Sheet

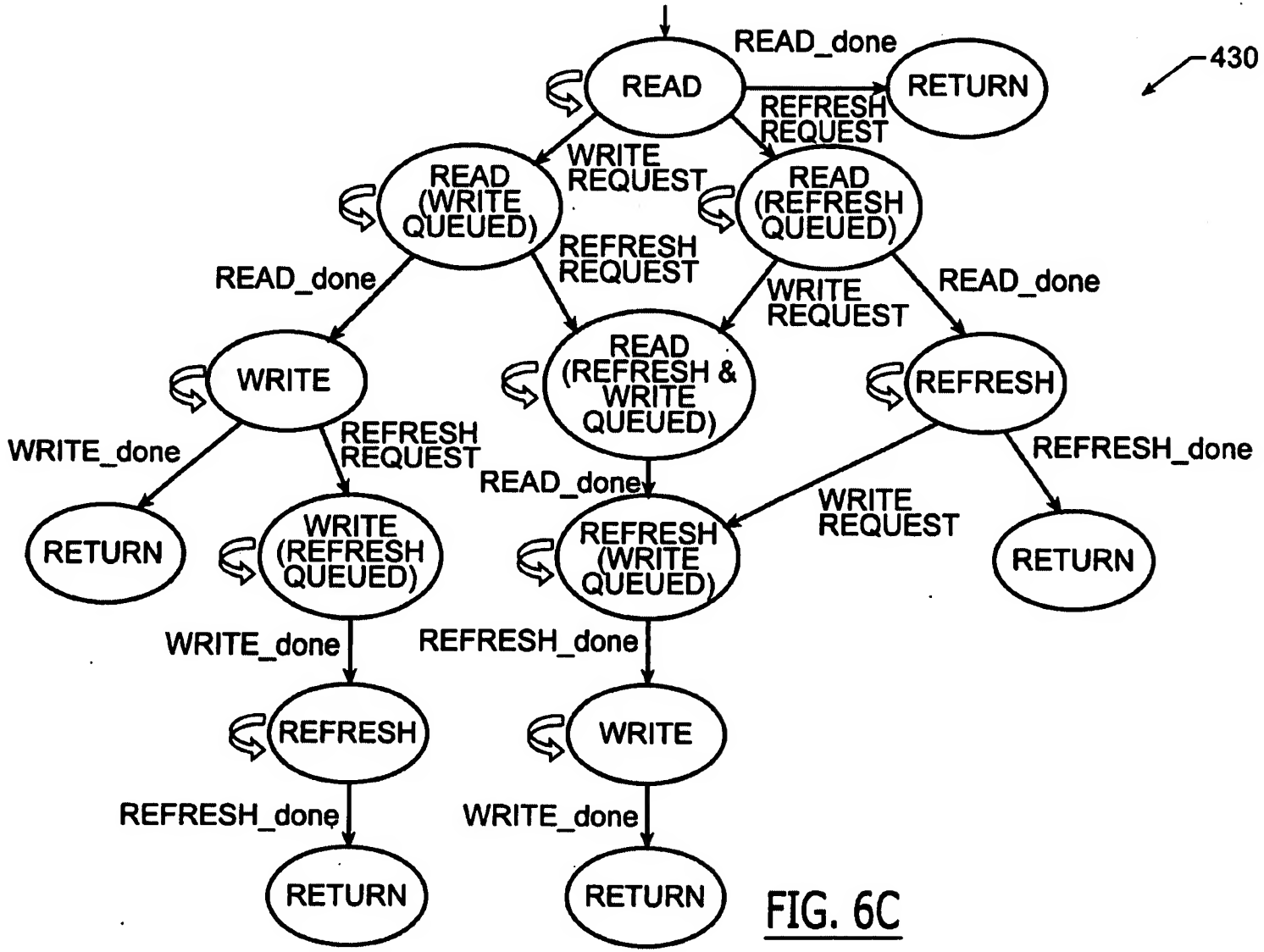


FIG. 6C

Replacement Sheet

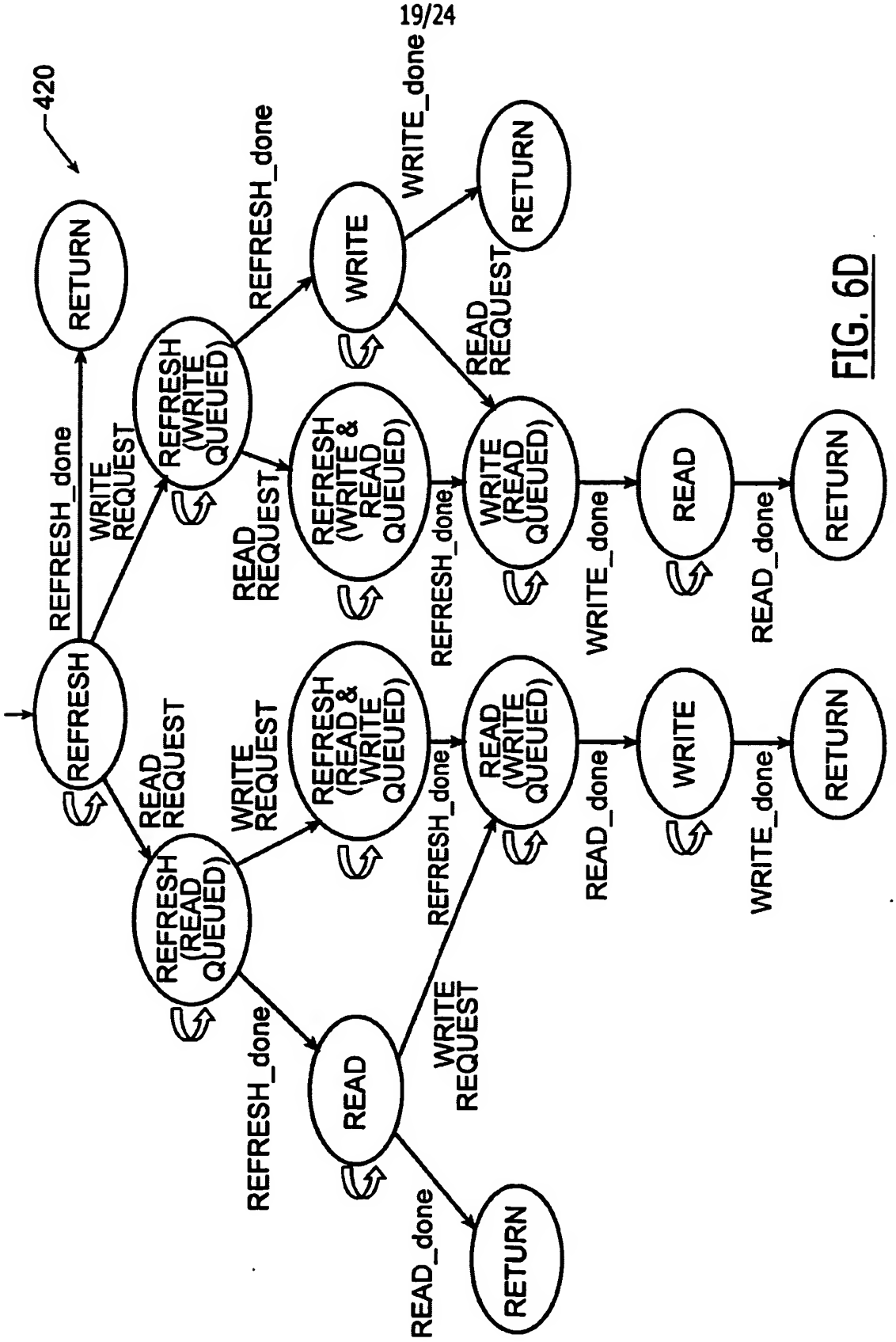

420
REFRESH
RETURN
REFRESH_done
WRITE REQUEST
READ REQUEST
REFRESH (READ QUEUED)
REFRESH (WRITE QUEUED)
REFRESH (READ & WRITE QUEUED)
REFRESH (WRITE & READ QUEUED)
READ
WRITE
READ (WRITE QUEUED)
WRITE (READ QUEUED)
READ_done
WRITE_done
RETURN

FIG. 6D

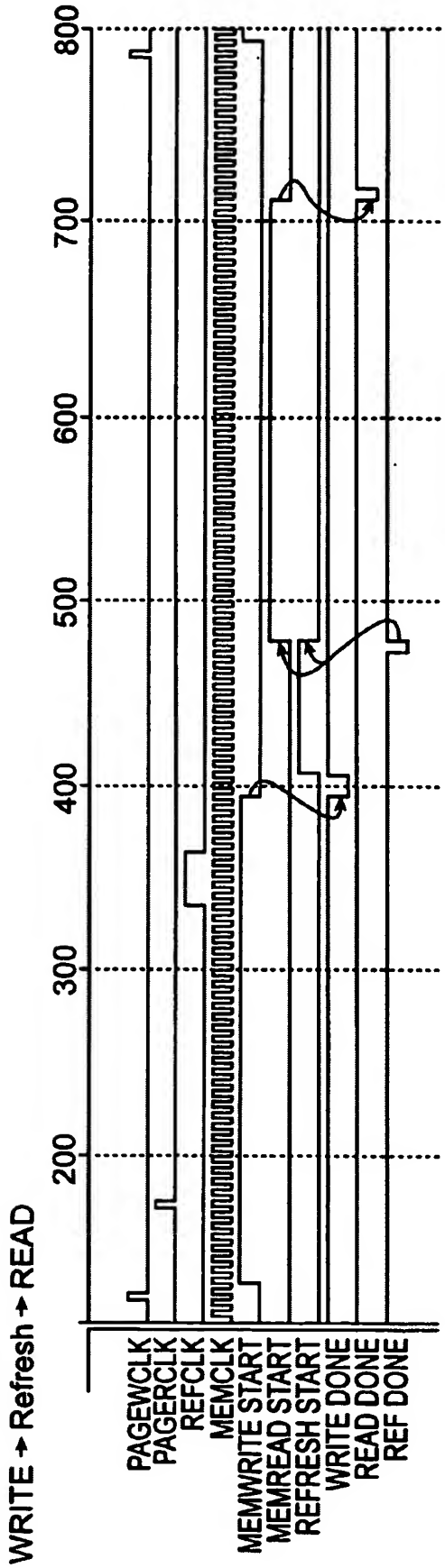

WRITE → Refresh → READ
200
300
400
500
600
700
800
PAGEWCLK
PAGERCLK
REFCLK
MEMCLK
MEMWRITE START
MEMREAD START
REFRESH START
WRITE DONE
READ DONE
REF DONE

FIG. 7A

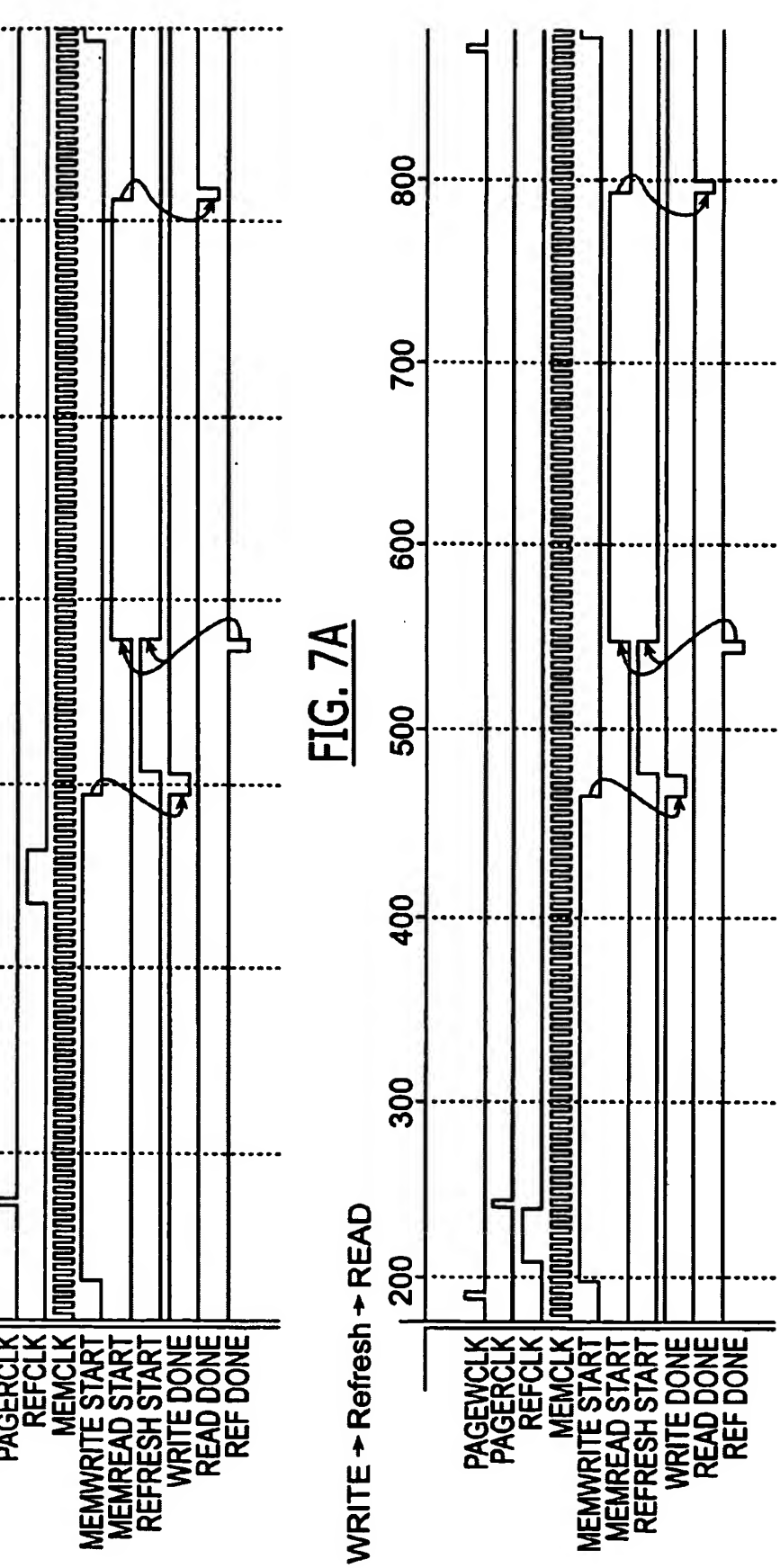

WRITE → Refresh → READ
200
300
400
500
600
700
800
PAGEWCLK
PAGERCLK
REFCLK
MEMCLK
MEMWRITE START
MEMREAD START
REFRESH START
WRITE DONE
READ DONE
REF DONE

FIG. 7B

WRITE → READ → Refresh

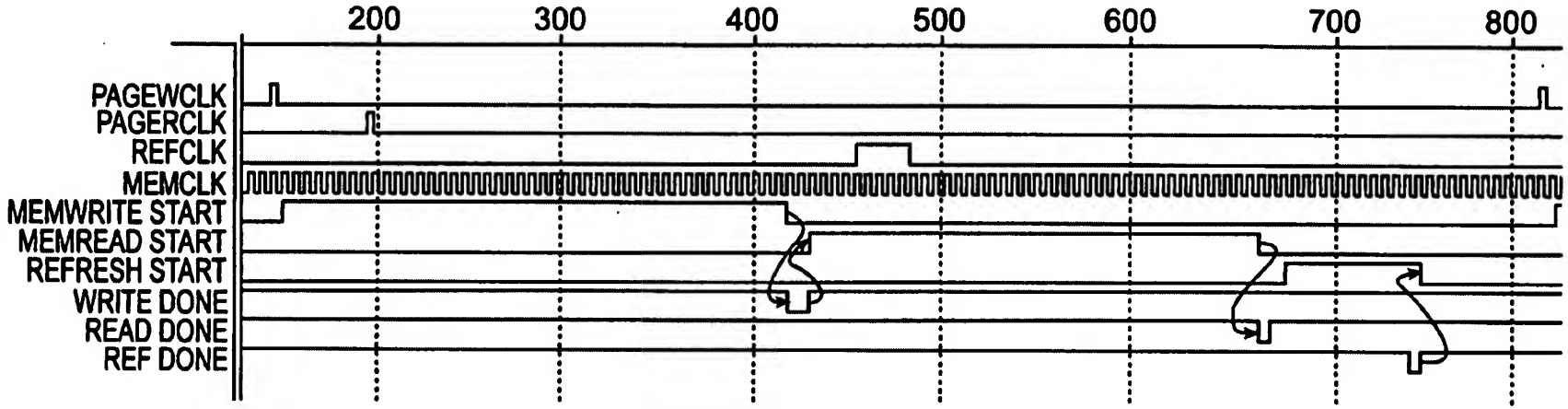


FIG. 7C

READ → Refresh → WRITE

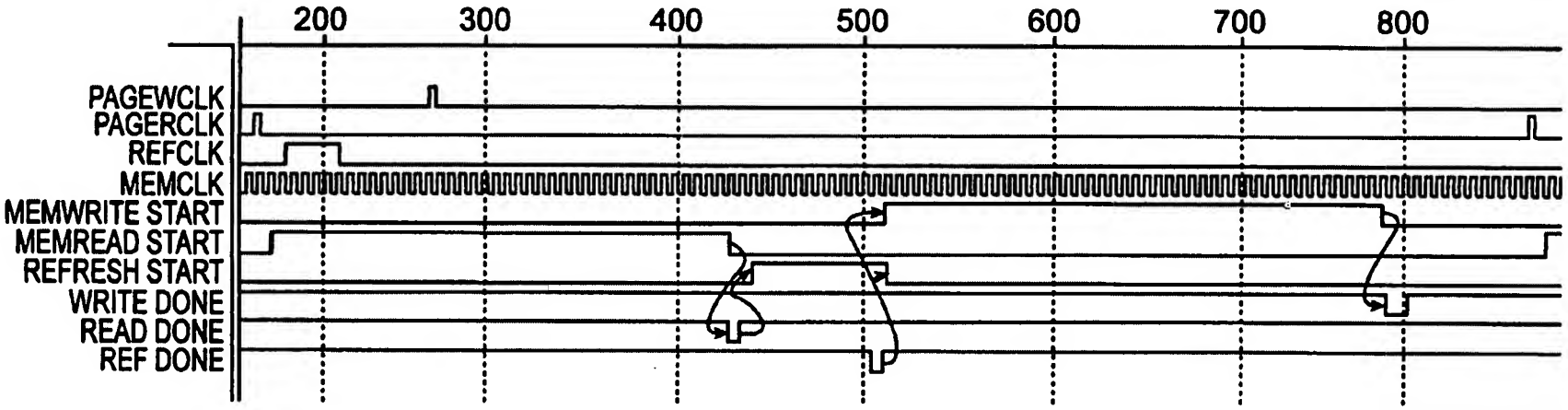


FIG. 7D

Replacement Sheet

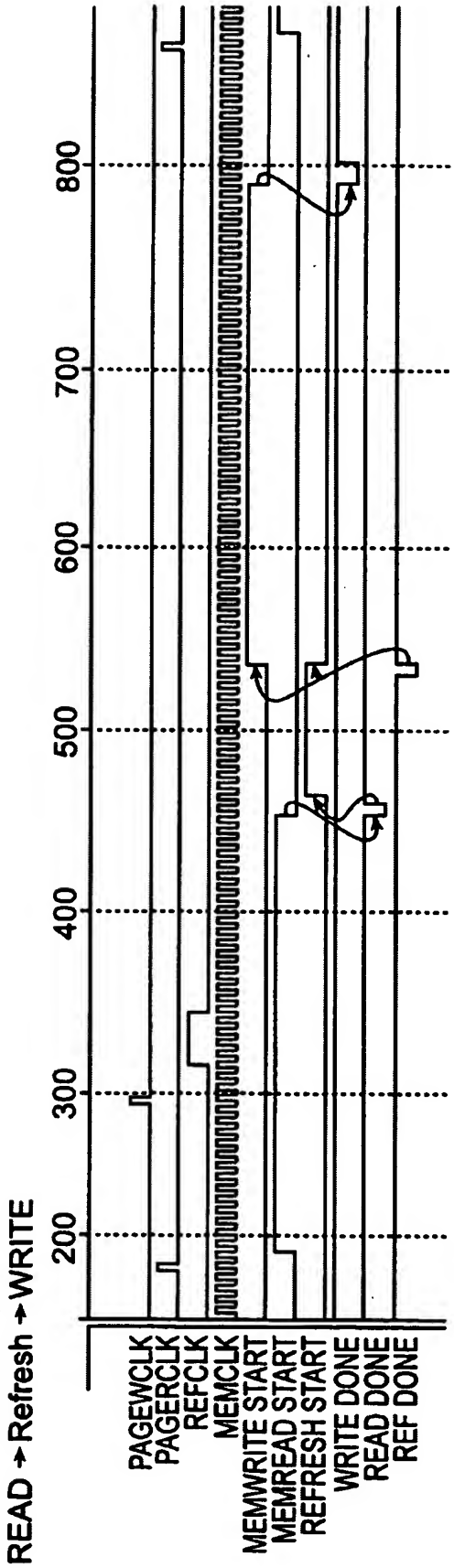

READ → Refresh → WRITE
200
300
400
500
600
700
800
PAGEWCLK
PAGERCLK
REFCLK
MEMCLK
MEMWRITE START
MEMREAD START
REFRESH START
WRITE DONE
READ DONE
REF DONE

FIG. 7E

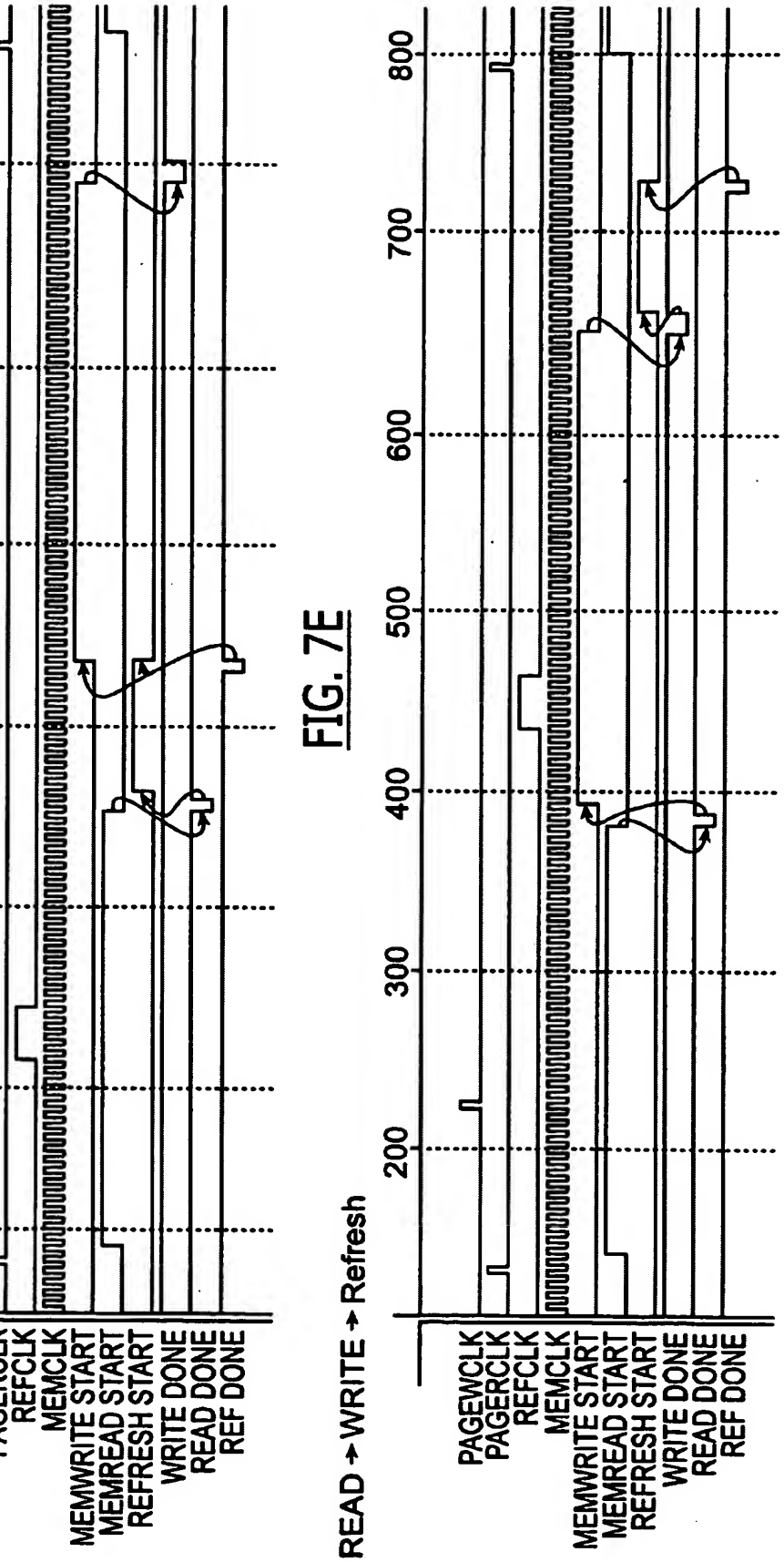

READ → WRITE → Refresh
200
300
400
500
600
700
800
PAGEWCLK
PAGERCLK
REFCLK
MEMCLK
MEMWRITE START
MEMREAD START
REFRESH START
WRITE DONE
READ DONE
REF DONE

FIG. 7F

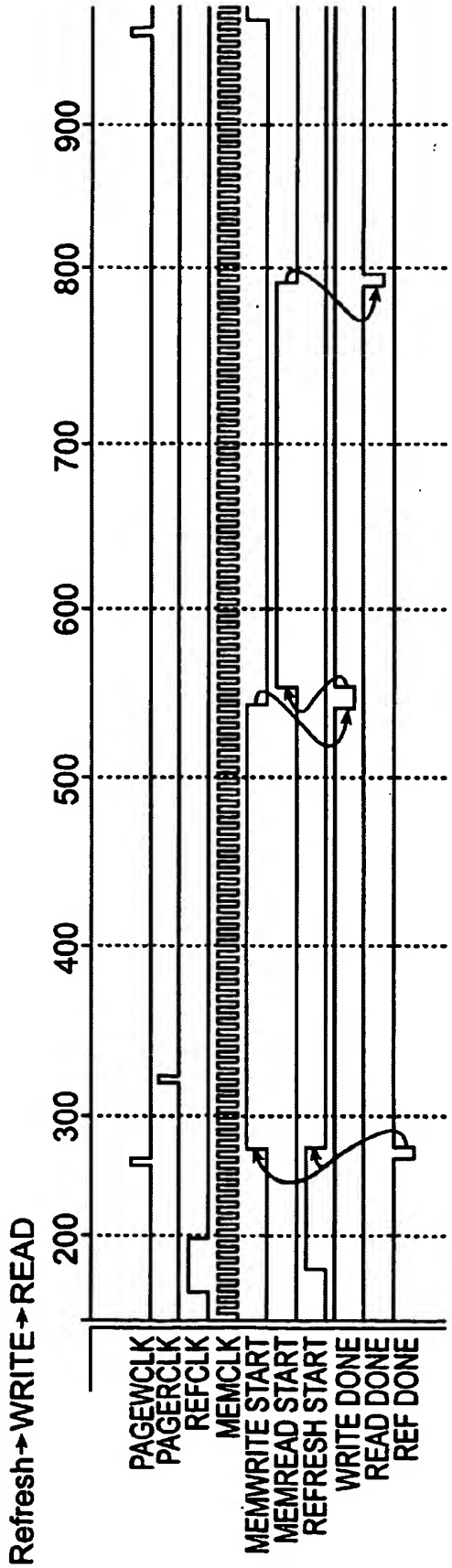

Refresh→WRITE→READ
200
300
400
500
600
700
800
900
PAGEWCLK
PAGERCLK
REFCLK
MEMCLK
MEMWRITE START
MEMREAD START
REFRESH START
WRITE DONE
READ DONE
REF DONE

FIG. 7G

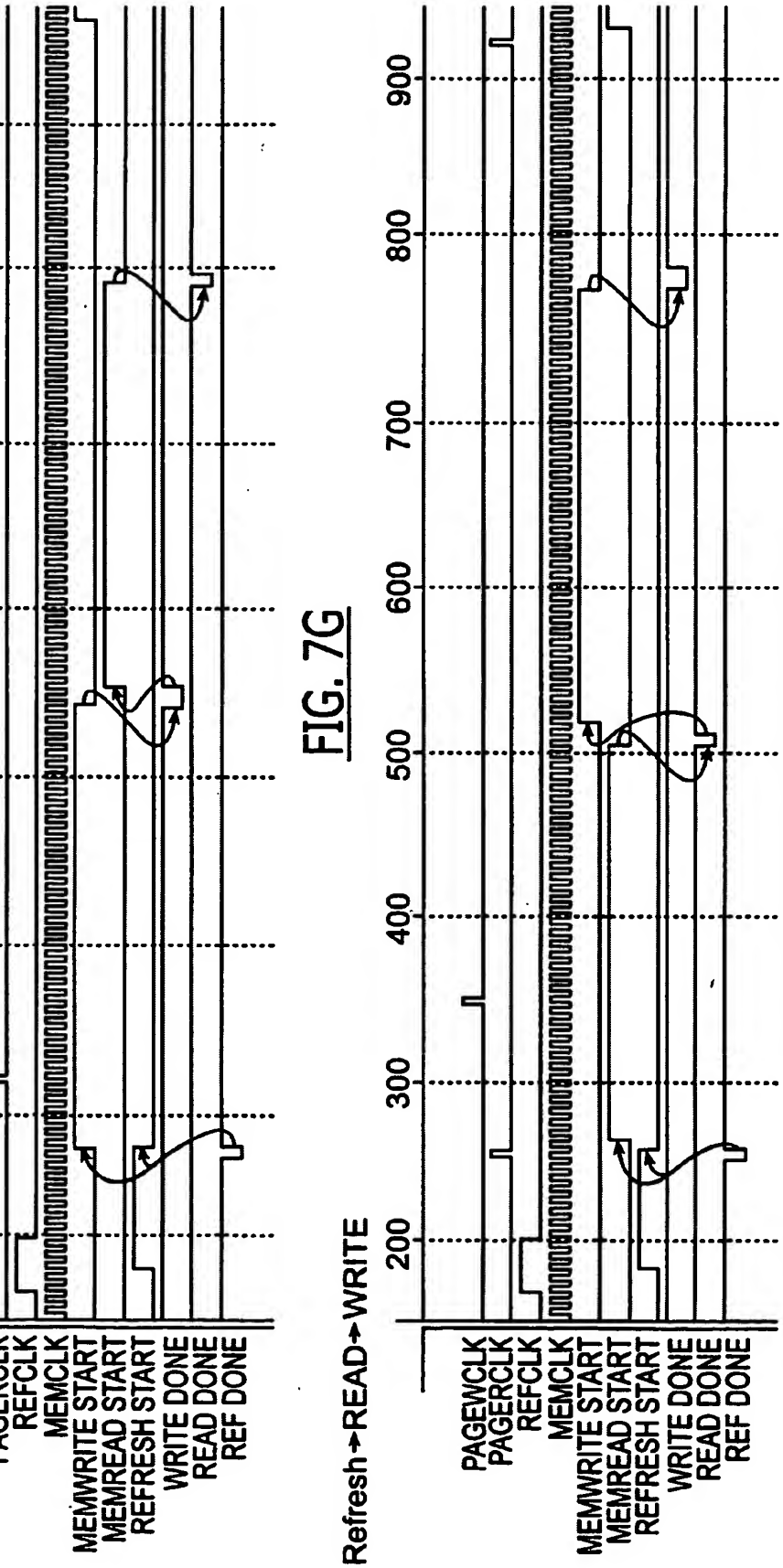

Refresh→READ→WRITE
200
300
400
500
600
700
800
900
PAGEWCLK
PAGERCLK
REFCLK
MEMCLK
MEMWRITE START
MEMREAD START
REFRESH START
WRITE DONE
READ DONE
REF DONE

FIG. 7H

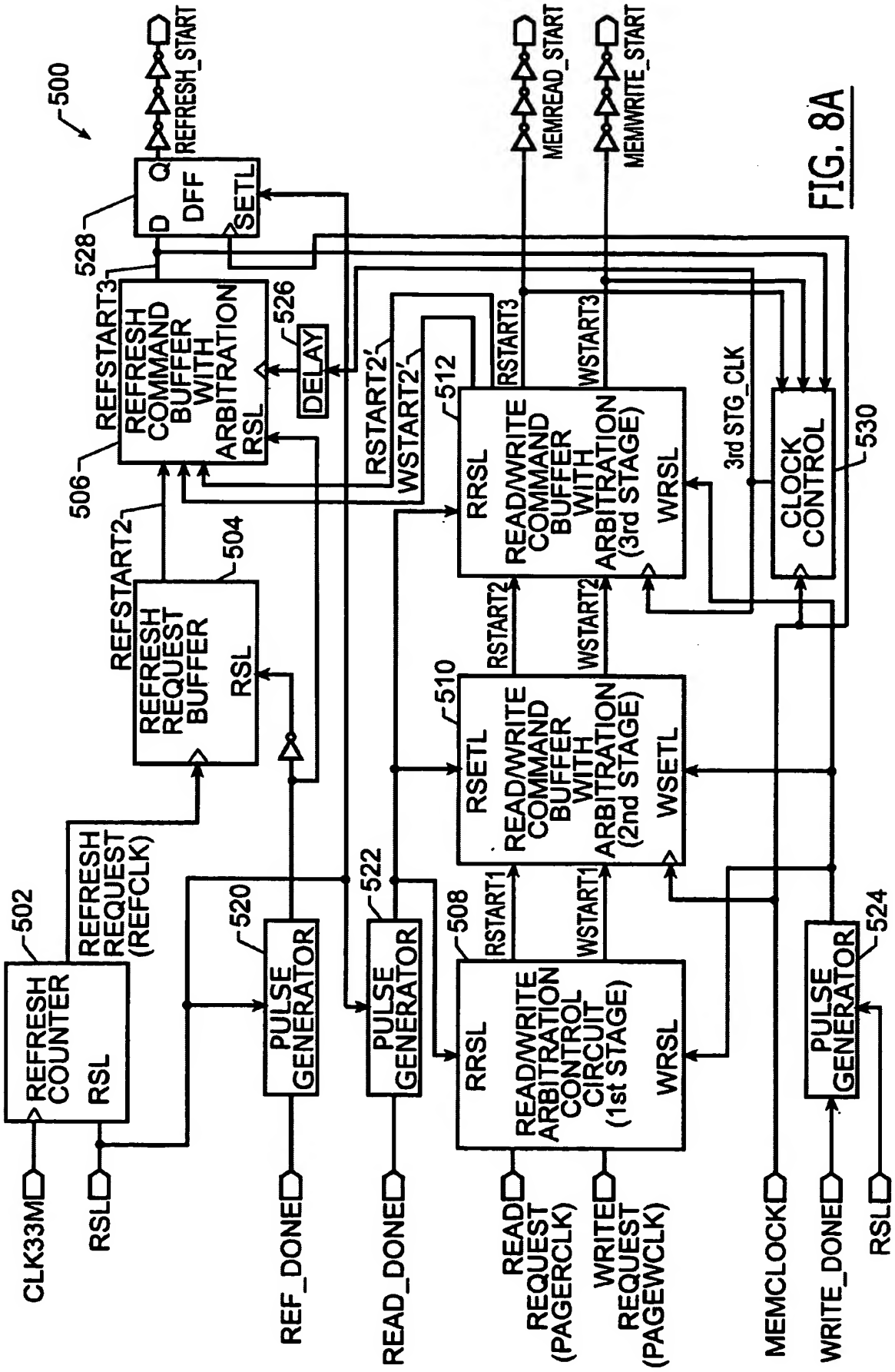

500
REFRESH_START
MEMREAD_START
MEMWRITE_START
D
Q
DFF
SETL
528
REFSTART3
REFRESH COMMAND BUFFER WITH ARBITRATION
RSL
526
DELAY
506
REFSTART2
504
REFRESH REQUEST BUFFER
RSL
RSTART2'
WSTART2'
512
RSTART3
WSTART3
RRSL
READ/WRITE COMMAND BUFFER WITH ARBITRATION (3rd STAGE)
WRSL
3rd STG_CLK
CLOCK CONTROL
530
RSTART2
WSTART2
510
RSETL
READ/WRITE COMMAND BUFFER WITH ARBITRATION (2nd STAGE)
WSETL
502
REFRESH COUNTER
RSL
REFRESH REQUEST (REFCLK)
520
PULSE GENERATOR
522
PULSE GENERATOR
RSTART1
WSTART1
508
RRSL
READ/WRITE ARBITRATION CONTROL CIRCUIT (1st STAGE)
WRSL
524
PULSE GENERATOR
CLK33M
RSL
REF_DONE
READ_DONE
READ REQUEST (PAGERCLK)
WRITE REQUEST (PAGEWCLK)
MEMCLOCK
WRITE_DONE
RSL

FIG. 8A

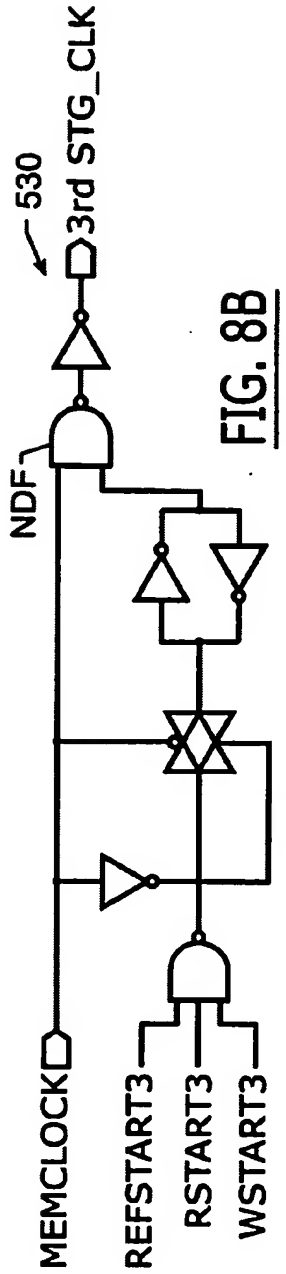


FIG. 8B

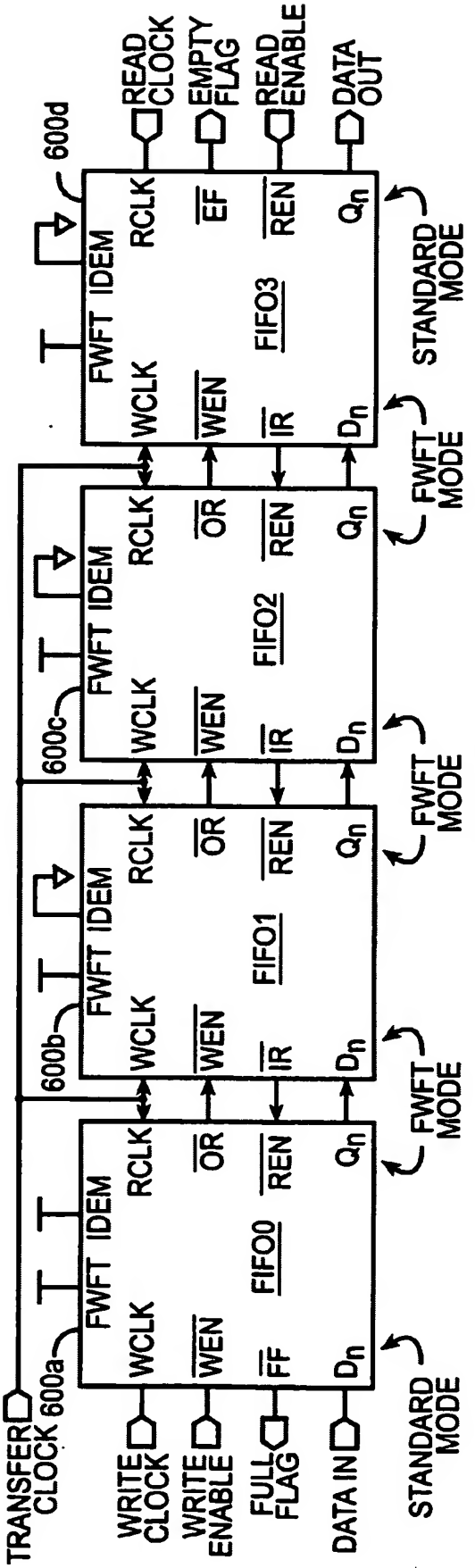

600
600a
600b
600c
600d
FWFT IDEM
WCLK
RCLK
WEN
REN
OR
IR
EF
FF
Dn
Qn
FIFO0
FIFO1
FIFO2
FIFO3
TRANSFER CLOCK
WRITE CLOCK
WRITE ENABLE
FULL FLAG
DATA IN
READ CLOCK
EMPTY FLAG
READ ENABLE
DATA OUT
STANDARD MODE
FWFT MODE

FIG. 9A

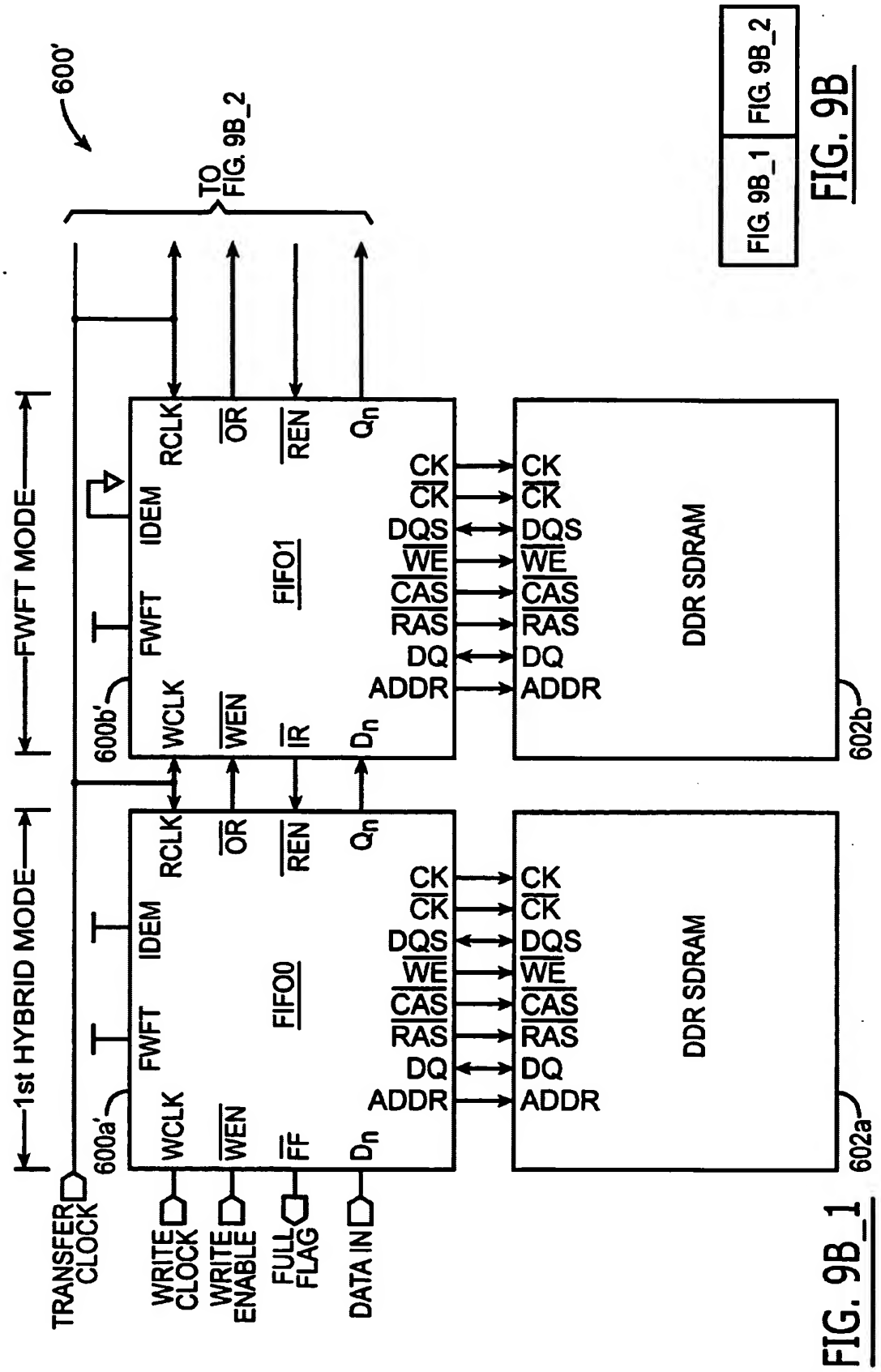


FIG. 9B_1

FIG. 9B

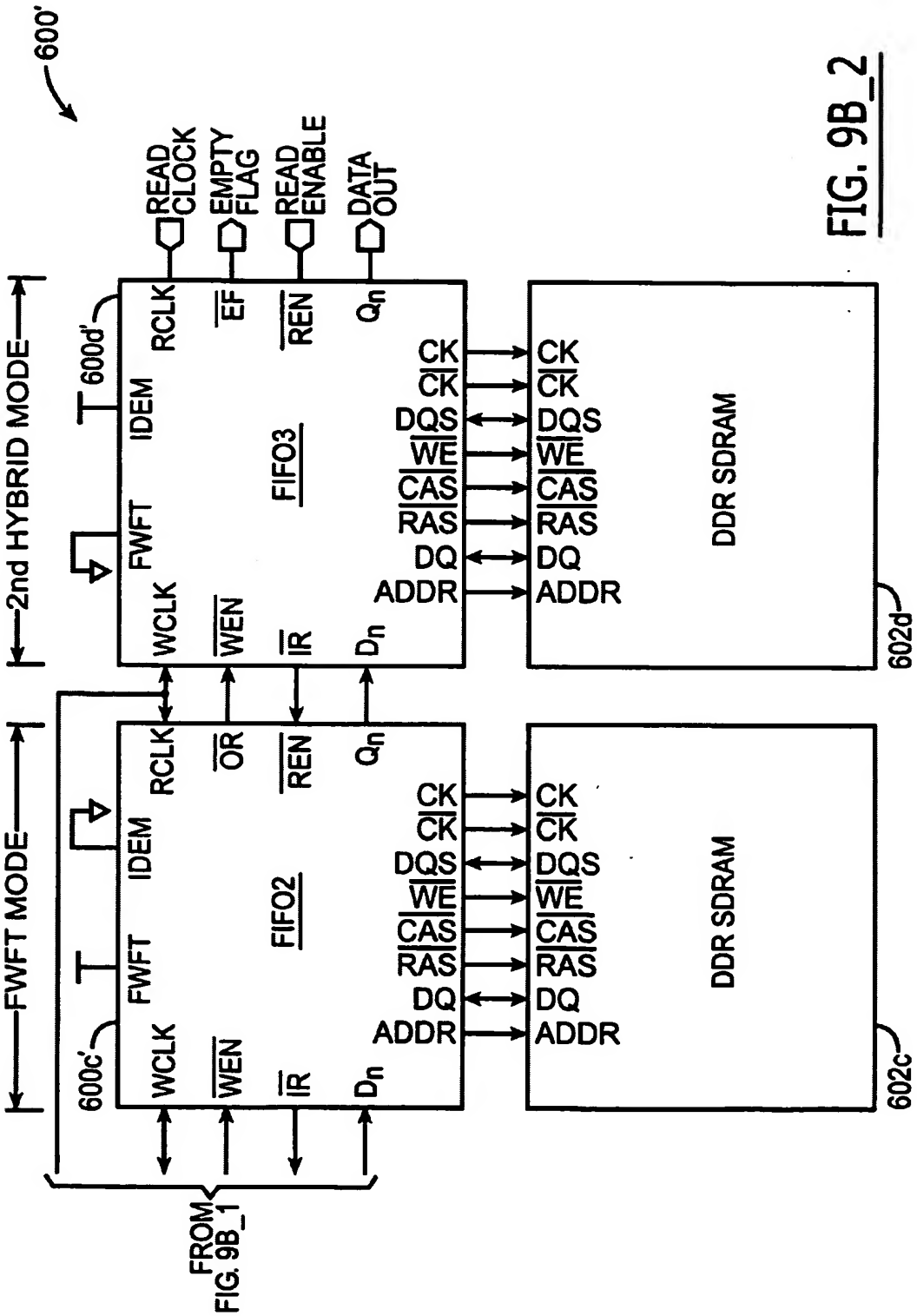

600'
READ CLOCK
EMPTY FLAG
READ ENABLE
DATA OUT
2nd HYBRID MODE
600d'
RCLK
EF
REN
Qn
IDEM
FIFO3
FWFT
WCLK
WEN
IR
Dn
CK
CK
DQS
WE
CAS
RAS
DQ
ADDR
DDR SDRAM
602d
FWFT MODE
600c'
OR
FIFO2
602c
FROM FIG. 9B_1

FIG. 9B_2